CLAIMS

1. A method for manufacturing a thin film integrated circuit, comprising the steps of:

forming a separation layer over an insulating substrate;

forming at least two thin film integrated circuits over the separation layer;

forming a groove between the two thin film integrated circuits to expose the separation layer;

attaching an antenna substrate provided with an opening and an antenna over the two thin film integrated circuits; and

separating the insulating substrate by introducing an etchant into the opening and removing the separation layer,

wherein the two thin film integrated circuits are integrated by the antenna substrate.

2. A method for manufacturing a thin film integrated circuit, comprising the steps of:

forming a separation layer over an insulating substrate;

forming at least two thin film integrated circuits over the separation layer;

selectively forming a groove between the two thin film integrated circuits to expose a part of the separation layer and form a connection region which is a part of the two thin film integrated circuits; and

separating the insulating substrate by introducing an etchant into the opening and removing the separation layer,

wherein the two thin film integrated circuits are integrated by the connection region.

3. A method for manufacturing a thin film integrated circuit, comprising the steps of:

forming a separation layer over an insulating substrate;

forming at least two thin film integrated circuits over the separation layer;

selectively forming a groove between the two thin film integrated circuits to expose a part of the separation layer and form a connection region which is a part of the two thin film integrated circuits;

attaching an antenna substrate provided with an opening and an antenna over the two thin film integrated circuits; and

separating the insulating substrate by introducing an etchant into the groove and the opening and removing the separation layer,

wherein the two thin film integrated circuits are integrated by the antenna substrate.

4. The method for manufacturing a thin film integrated circuit according to claim 1, further comprising the steps of:

attaching the two thin film integrated circuits to a flexible substrate.

5. The method for manufacturing a thin film integrated circuit according to claim 2, further comprising the steps of:

attaching an antenna to the two thin film integrated circuits.

6. The method for manufacturing a thin film integrated circuit according to claim 2, further comprising the steps of:

attaching an antenna to the two thin film integrated circuits; and

attaching the two thin film integrated circuits to a flexible substrate.

7. The method for manufacturing a thin film integrated circuit according to claim 3, further comprising the steps of:

attaching the two thin film integrated circuits to a flexible substrate.

8. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein each of the two thin film integrated circuits comprises a thin film transistor and an insulating film containing nitrogen provided over and under the thin film

transistor.

9. The method for manufacturing a thin film integrated circuit according to claim 2,

wherein each of the thin film integrated circuits comprises a thin film transistor and an insulating film containing nitrogen provided over and under the thin film transistor.

10. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein each of the thin film integrated circuits comprises a thin film transistor and an insulating film containing nitrogen provided over and under the thin film transistor.

11. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein the etchant is a gas or a liquid including halide typified by ClF_3.

12. The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the etchant is a gas or a liquid including halide typified by ClF_3.

13. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the etchant is a gas or a liquid including halide typified by ClF_3.

14. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein the insulating substrate is a glass substrate, a quartz substrate, or a substrate made of a synthetic resin such as plastic or acrylic.

15. The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the insulating substrate is a glass substrate, a quartz substrate, or a substrate made of a synthetic resin such as plastic or acrylic.

16. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the insulating substrate is a glass substrate, a quartz substrate, or a substrate made of a synthetic resin such as plastic or acrylic.

17. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein a mounting position of each of the two thin film integrated circuits X satisfies $(1/2)\cdot D-30\ \mu m<X<(1/2)\cdot D+30\ \mu m$ when a thickness of a mount article is denoted by D.

18. The method for manufacturing a thin film integrated circuit according to claim 2,

wherein a mounting position of each of the two thin film integrated circuits X satisfies $(1/2)\cdot D-30\ \mu m<X<(1/2)\cdot D+30\ \mu m$ when a thickness of a mount article is denoted by D.

19. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein a mounting position of each of the two thin film integrated circuits X satisfies $(1/2)\cdot D-30\ \mu m<X<(1/2)\cdot D+30\ \mu m$ when a thickness of a mount article is denoted by D.

20. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein the antenna is attached to the two thin film integrated circuits by an anisotropic conductor, an ultrasonic adhesive, or an ultraviolet curing resin.

21. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the antenna is attached to the two thin film integrated circuits by an anisotropic conductor, an ultrasonic adhesive, or an ultraviolet curing resin.

22. The method for manufacturing a thin film integrated circuit according to claim 5,

wherein the antenna is attached to the two thin film integrated circuits by an anisotropic conductor, an ultrasonic adhesive, or an ultraviolet curing resin.

23. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein the antenna is formed by a method selected from the group consisting of a droplet discharge method, a sputtering method, a printing method, a plating method, a photolithography method, an evaporation method using a metal mask, and a combination thereof.

24. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the antenna is formed by a method selected from the group consisting of a droplet discharge method, a sputtering method, a printing method, a plating method, a photolithography method, an evaporation method using a metal mask, and a combination thereof.

25. The method for manufacturing a thin film integrated circuit according to claim 5,

wherein the antenna is formed by a method selected from the group consisting of a droplet discharge method, a sputtering method, a printing method, a plating method, a photolithography method, an evaporation method using a metal mask, and a combination thereof.

26. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein the separation layer is an amorphous semiconductor, a semi-amorphous semiconductor, a microcrystalline semiconductor, or a crystalline semiconductor.

27. The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the separation layer is an amorphous semiconductor, a semi-amorphous semiconductor, a microcrystalline semiconductor, or a crystalline semiconductor.

28. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the separation layer is an amorphous semiconductor, a semi-amorphous semiconductor, a microcrystalline semiconductor, or a crystalline semiconductor.

29. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein the two thin film integrated circuits have a thickness of 0.3 μm to 3 μm.

30. The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the two thin film integrated circuits have a thickness of 0.3 μm to 3 μm.

31. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the two thin film integrated circuits have a thickness of 0.3 μm to 3 μm.

32. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein the two thin film integrated circuits are 5 mm squared or less.

33. The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the two thin film integrated circuits are 5 mm squared or less.

34. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the two thin film integrated circuits are 5 mm squared or less.

35. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein each of the two thin film integrated circuits includes a semiconductor film having a hydrogen concentration of 1×10^{19} /cm^3 to 5×10^{20} /cm^3.

36. The method for manufacturing a thin film integrated circuit according to claim 2,

wherein each of the two thin film integrated circuits includes a semiconductor film having a hydrogen concentration of 1×10^{19} /cm^3 to 5×10^{20} /cm^3.

37. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein each of the two thin film integrated circuits includes a semiconductor film having a hydrogen concentration of 1×10^{19} /cm^3 to 5×10^{20} /cm^3.

38. The method for manufacturing a thin film integrated circuit according to claim 35,

wherein the semiconductor film has a thickness of 0.2 μm or less.

39. The method for manufacturing a thin film integrated circuit according to claim 36,

wherein the semiconductor film has a thickness of 0.2 μm or less.

40. The method for manufacturing a thin film integrated circuit according to claim 37,

wherein the semiconductor film has a thickness of 0.2 μm or less.

41. The method for manufacturing a thin film integrated circuit according to claim 35,

wherein the semiconductor film comprises a source region, a drain region, and a channel formation region and,

wherein the source region, the drain region, and the channel formation region are formed to be perpendicular to a bending direction of a mount article.

42. The method for manufacturing a thin film integrated circuit according to claim 36,

wherein the semiconductor film comprises a source region, a drain region, and a channel formation region and,

wherein the source region, the drain region, and the channel formation region are formed to be perpendicular to a bending direction of a mount article.

43. The method for manufacturing a thin film integrated circuit according to claim 37,

wherein the semiconductor film comprises a source region, a drain region, and a channel formation region and,

wherein the source region, the drain region, and the channel formation region are formed to be perpendicular to a bending direction of a mount article.

44. The method for manufacturing a thin film integrated circuit according to claim 1,

wherein a thin film integrated circuit is formed by cutting the two thin film integrated circuits by a dicing, a scribing, or a laser cutting method.

45. The method for manufacturing a thin film integrated circuit according to claim

2,

wherein a thin film integrated circuit is formed by cutting the two thin film integrated circuits by a dicing, a scribing, or a laser cutting method.

46. The method for manufacturing a thin film integrated circuit according to claim 3,

wherein a thin film integrated circuit is formed by cutting the two thin film integrated circuits by a dicing, a scribing, or a laser cutting method.

47. An element substrate comprising:

an insulating substrate;

a separation layer over the insulating substrate;

at least two thin film integrated circuits over the separation layer; and

an antenna substrate provided opposite to the insulating substrate,

wherein the antenna substrate includes an antenna and an opening, and

wherein a groove is provided between the two thin film integrated circuits to correspond to the opening.

48. An element substrate comprising:

an insulating substrate;

a separation layer over the insulating substrate;

at least two thin film integrated circuits over the separation layer;

a connection region; and

an antenna substrate provided opposite to the insulating substrate,

wherein the antenna substrate includes an antenna and a first opening,

wherein a groove is provided between the two thin film integrated circuits to correspond to the first opening,

wherein a second opening is provided in the two thin film integrated circuits, and

wherein the two thin film integrated circuits are integrated by the connection region.

49. The element substrate according to claim 47,

wherein each of the two thin film integrated circuits comprises a thin film transistor and a layer having an insulating film containing nitrogen provided over and under the two thin film integrated circuits.

50. The element substrate according to claim 48,

wherein each of the two thin film integrated circuits comprises a thin film transistor and a layer having an insulating film containing nitrogen provided over and under the two thin film integrated circuits.

51. The element substrate according to claim 47,

wherein the separation layer is an amorphous semiconductor, a semi-amorphous semiconductor, a microcrystalline semiconductor, or a crystalline semiconductor.

52. The element substrate according to claim 48,

wherein the separation layer is an amorphous semiconductor, a semi-amorphous semiconductor, a microcrystalline semiconductor, or a crystalline semiconductor.

53. The element substrate according to claim 47,

wherein the two thin film integrated circuits have a thickness of 0.3 μm to 3 μm.

54. The element substrate according to claim 48,

wherein the two thin film integrated circuits have a thickness of 0.3 μm to 3 μm.

55. The element substrate according to claim 47,

Wherein each of the two thin film integrated circuits includes a semiconductor film having a hydrogen concentration of 1×10^{19} /cm^3 to 5×10^{20} /cm^3.

56. The element substrate according to claim 48,

Wherein each of the two thin film integrated circuits includes a semiconductor film having a hydrogen concentration of 1×10^{19} /cm^3 to 5×10^{20} /cm^3.

57. The element substrate according to claim 55,
wherein the semiconductor film has a thickness of 0.2 μm or less.

58. The element substrate according to claim 56,
wherein the semiconductor film has a thickness of 0.2 μm or less.

59. The element substrate according to claim 47,
wherein the element substrate is mounted with a product selected from the group consisting of a label, a banknote, a check, a stock certificate and a card.

60. The element substrate according to claim 48,
wherein the element substrate is mounted with a product selected from the group consisting of a label, a banknote, a check, a stock certificate and a card.